Powerful Energy Meter Chipset

ADSST-SALEM-3T

FEATURES

High accuracy
Supports IEC 60687/61036 and ANSI C12.1/12.20
Suitable for class0.5 and class0.2 meter
Full four quadrant measurement of parameters
SPI® compatible serial interface
Pulse output with programmable pulse constant as pulses/kWh or Wh/pulse
Programmable duty cycle for pulse output
Embedded calibration routines for gain and dc offset
Software based phase and nonlinearity compensation for current transformers
15 kHz sampling frequency
UART mode enables a PC to directly access all computed parameters
Flags to indicate tamper conditions
Single 3.0 V supply
Developer's kit to accelerate design process (See Ordering Guide for separate ordering number.)

GENERAL DESCRIPTION

The ADSST-SALEM-3T energy meter chipset consists of an efficient ADSST-218x digital signal processor (DSP), a fast and accurate 6-channel, 16-bit ADSST-73360LAR sigma-delta analog-to-digital converter (ADC), and metering software. Two chipset versions are available to support differing ranges of operating temperature: The ADSST-EM-3040 chipset is rated at 0°C to 70°C for commercial applications, while the ADSST-EM-3041 chipset operates at –25°C to +85°C for industrial use.

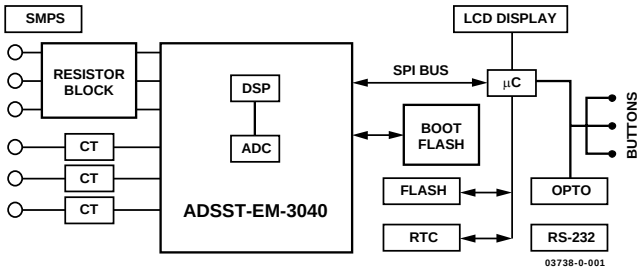

Figure 1. Block Diagram of a Functional Meter

The ADC and DSP are interfaced to simultaneously acquire voltage and current samples on all three phases and to perform mathematically intensive computations to calculate various instantaneous parameters and perform harmonic analysis. The chipset can be interfaced to any general-purpose microprocessor to develop state of the art tri-vector or polyphase energy metering solutions with a wide range of basic currents from 1 A to 30 A. By incorporating a comprehensive data set of parameters, including instantaneous measurements, accumulated parameters, and harmonic analysis data, the ADSST-SALEM-3T chipset meets high end energy metering requirements. The ability to easily configure the chipset for various parameters makes it a very flexible solution.

The phase and nonlinearity compensation for current transformers is done in software (patent pending) without having to use any passive components in the circuit for compensation, thus minimizing variations in accuracy with temperature and time.

The ADSST-SALEM-3T measures and computes a large number of parameters essential for high end metering.

Table 1.

Parameter	Each Phase	Total
RMS Voltage	✓	
RMS Current	✓	
Active Power	✓	✓
Apparent Power	✓	✓
Inductive Reactive Power	✓	✓
Capacitive Reactive Power	✓	✓
Power Factor	✓	✓
Frequency		✓
Positive Active Energy	✓	✓
Negative Active Energy	✓	✓
Apparent Energy	✓	✓
Positive Inductive Reactive Energy	✓	✓
Negative Inductive Reactive Energy	✓	✓
Positive Capacitive Reactive Energy	✓	✓
Negative Capacitive Reactive Energy	✓	✓
Voltage Magnitude and Phase for All Odd Harmonics up to 21st Order	✓	✓
Current Magnitude and Phase for All Odd Harmonics up to 21st Order	✓	✓

The ADSST-SALEM-3T offers some excellent features that make the final meter cost-effective and easy to manufacture.

Rev. 0

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REVISION HISTORY

7/04—Revision 0: Initial Version

EASY CALIBRATION

The ADSST-SALEM-3T chipset has highly advanced calibration routines embedded into the software. Ease of calibration is the key feature in this chipset. By sending specific commands to the ADSST-SALEM-3T chipset, the dc offsets and gains for all voltage and current channels can be calibrated automatically. Active and reactive power calibration is also available for fine-tuning the errors.

The meter and calibration constants are stored in an external flash memory, and the lock/unlock calibration feature enables protection of the calibration constants. The ability to upgrade the firmware residing in the flash memory makes the meter adaptable to future needs.

EFFECTIVE PHASE COMPENSATION

The ADSST-SALEM-3T chipset employs an algorithm (patent pending) for phase compensation. The ADSST-SALEM-3T chipset based meter, which is very effective and user friendly, can be calibrated for phase compensation at three current points to cover the complete current range. This also reduces the cost of the end product by reducing the cost of the sensing elements, i.e., current transformers.

EASE OF DESIGN

Designing a complete meter using the ADSST-SALEM-3T is very easy with the ADSST-SALEM-3T-DK developer's kit. The kit in the UART mode enables a user to evaluate and test the computational element by connecting to a PC, without building the complete hardware.

QUADRANT AND OTHER CONVENTIONS

The metering data computed by the ADSST-SALEM-3T chipset uses the following conventions for various parameters:

- Figure 2 gives the quadrant conventions used by the chipset.
- Import means power delivered from the utility to the user.
- Export means power delivered by the user to the utility.
- Total means total of all three phases.

Import and export are with reference to consumption.

U, I: Magnitude of voltage and current
P: Active Power ($U \times I \times \cos \Phi$)
Q: Reactive Power ($U \times I \times \sin \Phi$)
Φ: Phase angle from the standpoint of I with respect to U, always positive in counterclockwise direction.
Phase U: L1 = 0° Abs
L2 = 240° Abs
L3 = 120° Abs

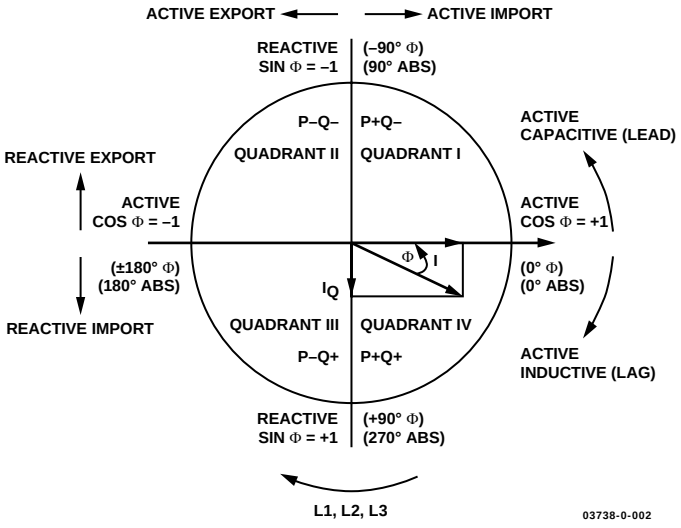

Figure 2. Quadrant Conventions

GENERAL DESCRIPTION OF THE ADSST-218X DSP

The ADSST-218x is a single-chip microcomputer optimized for digital signal processing (DSP) and other high speed numeric processing applications.

The DSP combines the ADSP-2100 family base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

The ADSST-218x is fabricated in a high speed, low power CMOS process. Every instruction can execute in a single processor cycle.

The ADSST-218x's flexible architecture and comprehensive instruction set enable the processor to perform multiple operations in parallel. In one processor cycle, the ADSST-218x can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

ARCHITECTURE OVERVIEW

The ADSST-218x instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSST-218x assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Figure 3 is the functional block diagram of the ADSST-218x. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations.

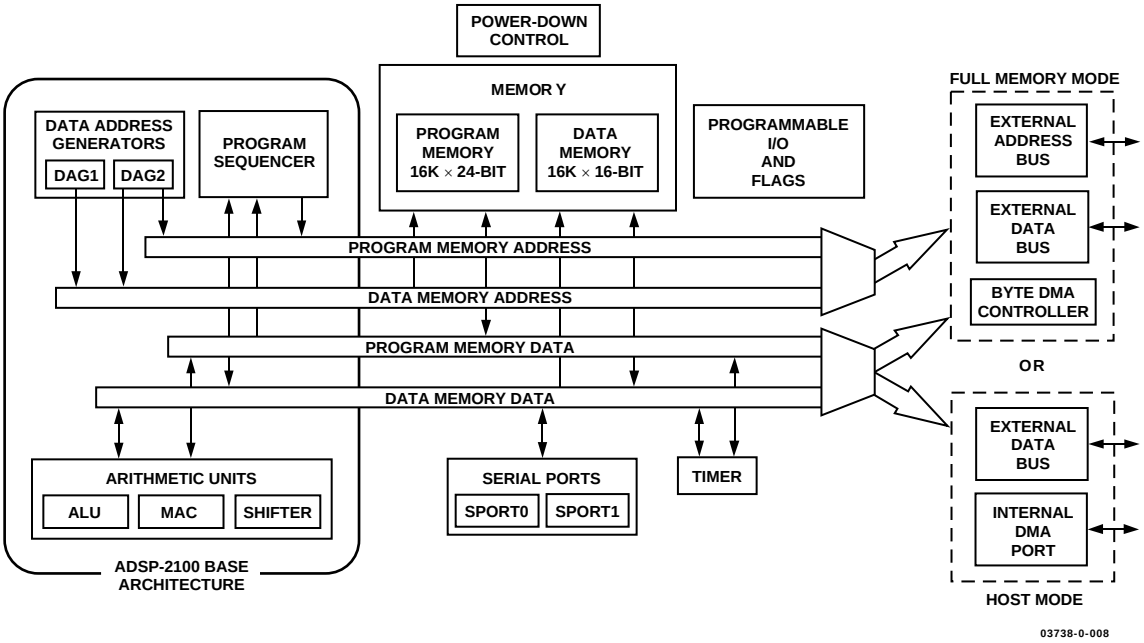

Figure 3. Functional Block Diagram

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG0}$). One execution mode (go mode) enables the ADSST-218x to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSST-218x can respond to 11 interrupts. There are up to six external interrupts (one edge sensitive, two level sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the byte $\overline{DMA}$ port, and the power-down circuitry. There is also a master $\overline{RESET}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Serial Ports

The ADSST-218x incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Package Description

The ADSST-218x is available in a 100-lead low profile quad flat package (LQFP, refer to Figure 5).

ADSST-218X COMMON-MODE PINS

Table 2.

Pin Name	No. of Pins	I/O	Function
$\overline{BG}$	1	O	Bus Grant Output
$\overline{BGH}$	1	O	Bus Grant Hung Output
$\overline{BMS}$	1	O	Byte Memory Select Output
$\overline{BR}$	1	I	Bus Request Input
$\overline{CMS}$	1	O	Combined Memory Select Output
$\overline{DMS}$	1	O	Data Memory Select Output
$\overline{IOMS}$	1	O	Memory Select Output
$\overline{PMS}$	1	O	Program Memory Select Output
$\overline{RD}$	1	O	Memory Read Enable Output
$\overline{RESET}$	1	I	Processor Reset Input
$\overline{WR}$	1	O	Memory Write Enable Output
$\overline{IRQ2}$/	1	I	Edge- or Level-Sensitive Interrupt Request[1]
PF7		I/O	Programmable I/O Pin
$\overline{IRQL1}$/	1	I	Level-Sensitive Interrupt Requests[1]
PF6		I/O	Programmable I/O Pin
$\overline{IRQL0}$/	1	I	Level-Sensitive Interrupt Requests[1]
PF5		I/O	Programmable I/O Pin
$\overline{IRQE}$/	1	I	Edge-Sensitive Interrupt Requests[1]
PF4		I/O	Programmable I/O Pin
MODE A	1	I	Mode Select Input–Checked only during $\overline{RESET}$
PF0		I/O	Programmable I/O Pin during Normal Operation
MODE B	1	I	Mode Select Input–Checked only during $\overline{RESET}$
PF1		I/O	Programmable I/O Pin during Normal Operation
MODE C	1	I	Mode Select Input–Checked only during $\overline{RESET}$
PF2		I/O	Programmable I/O Pin during Normal Operation
MODE D	1	I	Mode Select Input–Checked only during $\overline{RESET}$
PF3		I/O	Programmable I/O Pin during Normal Operation
CLKIN, XTAL	2	I	Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
EZ-Port	9	I/O	For Emulation Use
FI, FO			Flag In, Flag Out[2]
FL0, FL1, FL2	3	O	Output Flags
GND	10	I	Power and Ground
$\overline{IRQ1}$:0			Edge- or Level-Sensitive Interrupts
$\overline{PWD}$	1	I	Power-Down Control Input
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1	5	I/O	Serial Port I/O Pins
PWDACK	1	O	Power-Down Control Output
V_{DDEXT}	4	I	External V_{DD} (2.5 V or 3.3 V) Power (LQFP)
V_{DDEXT}	7	I	External V_{DD} (2.5 V or 3.3 V) Power (Mini-BGA)
V_{DDINT}	2	I	Internal V_{DD} (2.5 V) Power (LQFP)
V_{DDINT}	4	I	Internal V_{DD} (2.5 V) Power (Mini-BGA)

[1]Interrupt/flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices or set as a programmable flag.
[2]SPORT configuration determined by the DSP System Control register. Software configurable.

CLOCK SIGNALS

Either a crystal or a TTL compatible clock signal can clock the ADSST-218x.

If an external clock is used, it should be a TTL compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input must be left unconnected.

Because the ADSST-218x includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 4. The capacitor values are dependent on the crystal type and should be specified by the crystal manufacturer. A parallel resonant, fundamental frequency, microprocessor grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 autobuffer control register.

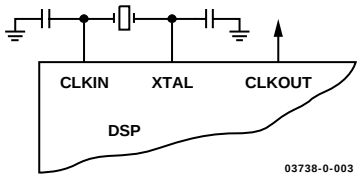

Figure 4. External Crystal Connections

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSST-2185x. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to enable the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence, the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse-width specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if an RC circuit is used to generate the $\overline{\text{RESET}}$ signal, the use of an external Schmitt trigger is recommended.

RECOMMENDED OPERATING CONDITIONS

Table 3.

Parameter	Min	Max	Unit
V_{DDINT}	2.37	2.63	V
V_{DDEXT}	2.37	3.60	V
V_{INPUT}[1]	V_{IL} = –0.3	V_{IH} = 3.6	V
T_{AMB}	0	70	°C

[1]The ADSST-2185x is 3.3 V tolerant (always accepts up to 3.6 V max V_{IH}), but voltage compliance (on output, V_{OH}) depends on the input V_{DDEXT}; because V_{OH} (MAX) = V_{DDEXT} (MAX). This applies to bidirectional pins (D0–D23, RFS0, $\overline{\text{RFS1}}$, SCLK0, SCLK1, $\overline{\text{TFS0}}$, A1–A13, PF0–PF7) and input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

ADSST-218X ELECTRICAL CHARACTERISTICS

Table 4.

Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH} High Level Input Voltage[1, 2]	@ V_{DDINT} = Max	1.5			V
V_{IH} High Level CLKIN Voltage	@ V_{DDINT} = Max	2.0			V
V_{IL} Low Level Input Voltage[1, 3]	@ V_{DDINT} = Min			0.7	V
V_{OH} High Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = Min, I_{OH} = –0.5 mA	2.0			V
	@ V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
	@ V_{DDEXT} = Min, I_{OH} = –100 µA[6]	V_{DDEXT} – 0.3			V
V_{OL} Low Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = Min, I_{OL} = 2 mA			0.4	V
I_{IH} High Level Input Current[3]	@ V_{DDINT} = Max, V_{IN} = 3.6 V			10	µA
I_{IL} Low Level Input Current[3]	@ V_{DDINT} = Max, V_{IN} = 0 V			10	µA
I_{OZH} Three-State Leakage Current[7]	@ V_{DDEXT} = Max, V_{IN} = 3.6 V[8]			10	µA
I_{OZL} Three-State Leakage Current[7]	@ V_{DDEXT} = Max, V_{IN} = 0 V[8]			10	µA
I_{DD} Supply Current (Idle)[9]	@ V_{DDINT} = 2.5 V, t_{CK} = 15 ns		9		mA
	@ V_{DDINT} = 2.5 V, t_{CK} = 13.3 ns		10		mA
I_{DD} Supply Current (Dynamic)[10]	@ V_{DDINT} = 2.5 V, t_{CK} = 13.3 ns[11], T_{AMB} = +25°C		35		mA
	@ V_{DDINT} = 2.5 V, t_{CK} = 15 ns[11], T_{AMB} = +25°C		38		mA
I_{DD} Supply Current (Power-Down)[12]	@ V_{DDINT} = 2.5 V, T_{AMB} = +25°C in Lowest Power Mode		100		mA
C_I Input Pin Capacitance[3, 6]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = +25°C			8	pF
C_O Output Pin Capacitance[6, 7, 12, 13]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = +25°C			8	pF

[1]Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.
[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.
[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.
[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$.
[5]Although specified for TTL outputs, all ADSP-2186 outputs are CMOS compatible and will drive to V_{DDEXT} and GND, assuming no dc loads.
[6]Guaranteed but not tested.
[7]Three-statable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0–PF7.
[8]0 V on $\overline{\text{BR}}$.
[9]Idle refers to ADSST-218x state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
[10]I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (Types 1, 4, 5, 12, 13, 14), 30% are Type 2 and Type 6, and 20% are idle instructions.
[11]V_{IN} = 0 V and 3 V. For typical figures for supply currents, refer to the Power Dissipation section.
[12]Applies to LQFP package type.
[13]Output pin capacitance is the capacitive load for any three-stated output pin.

ABSOLUTE MAXIMUM RATINGS—ADSST-218X

Table 5.

	Rating	
Parameter	**Min**	**Max**
Internal Supply Voltage (V_{DDINT})	–0.3 V	+3.0 V
External Supply Voltage (V_{DDEXT})	–0.3 V	+4.0 V
Input Voltage[1]	–0.3 V	+4.0 V
Output Voltage Swing[2]	–0.5 V	V_{DDEXT} + 0.5 V
Operating Temperature Range	0°C	70°C
Storage Temperature Range	–65°C	+150°C

[1]Applies to bidirectional pins (D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7) and input-only pins (CLKIN, RESET, BR, DR0, DR1, PWD).
[2]Applies to output pins (BG, PMS, DMS, BMS, IOMS, CMS, RD, WR, PWDACK, A0, DT0, DT1, CLKOUT, FL2–FL0, BGH).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION—ADSST-218X

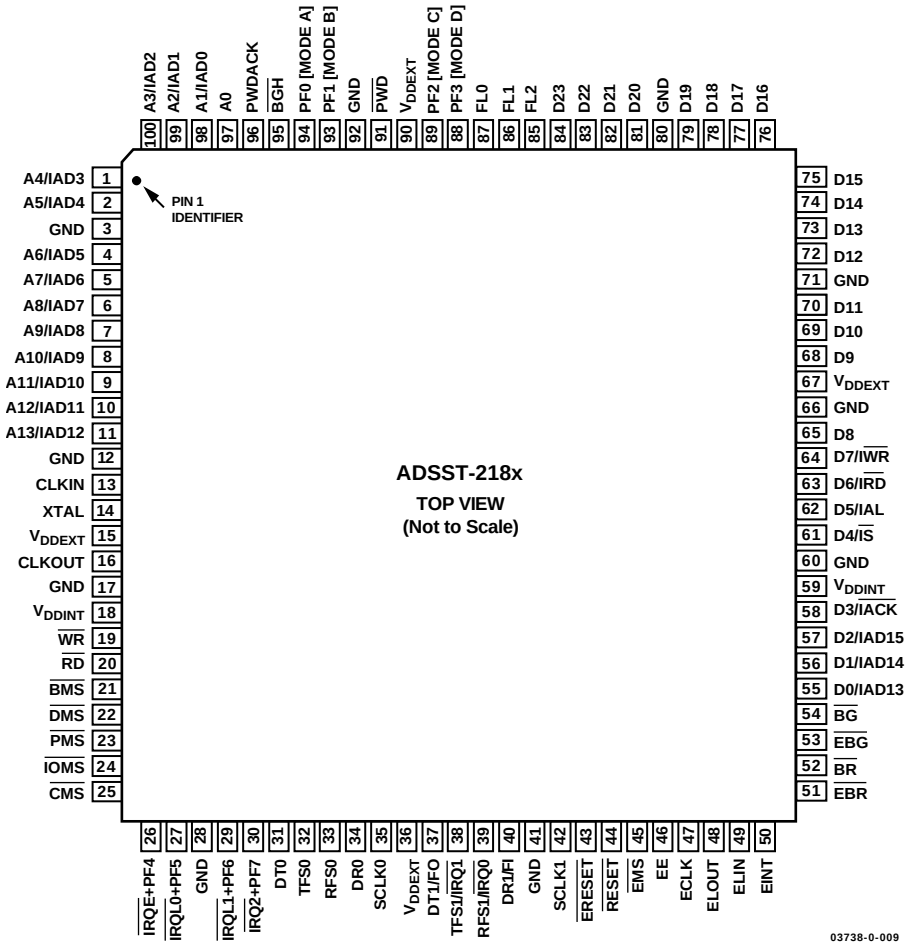

Figure 5. Pin Configuration for ADSST-218x in 100-Lead LQFP

GENERAL DESCRIPTION OF THE ADSST-73360LAR ADC

The ADSST-73360LAR is a 6-channel input analog front end processor for general-purpose applications, including industrial power metering or multichannel analog inputs. It features six 16-bit A/D conversion channels, each of which provides 76 dB signal-to-noise ratio over a dc to 4 kHz signal bandwidth. Each channel also features an input programmable gain amplifier (PGA) with gain settings in eight stages from 0 dB to 38 dB.

The ADSST-73360LAR is particularly suitable for industrial power metering as each channel samples synchronously, ensuring that there is no (phase) delay between the conversions. The ADSST-73360LAR also features low group delay conversions on all channels.

An on-chip reference voltage is included with a nominal value of 1.2 V.

The ADSST-73360LAR is available in a 28-lead SOIC package.

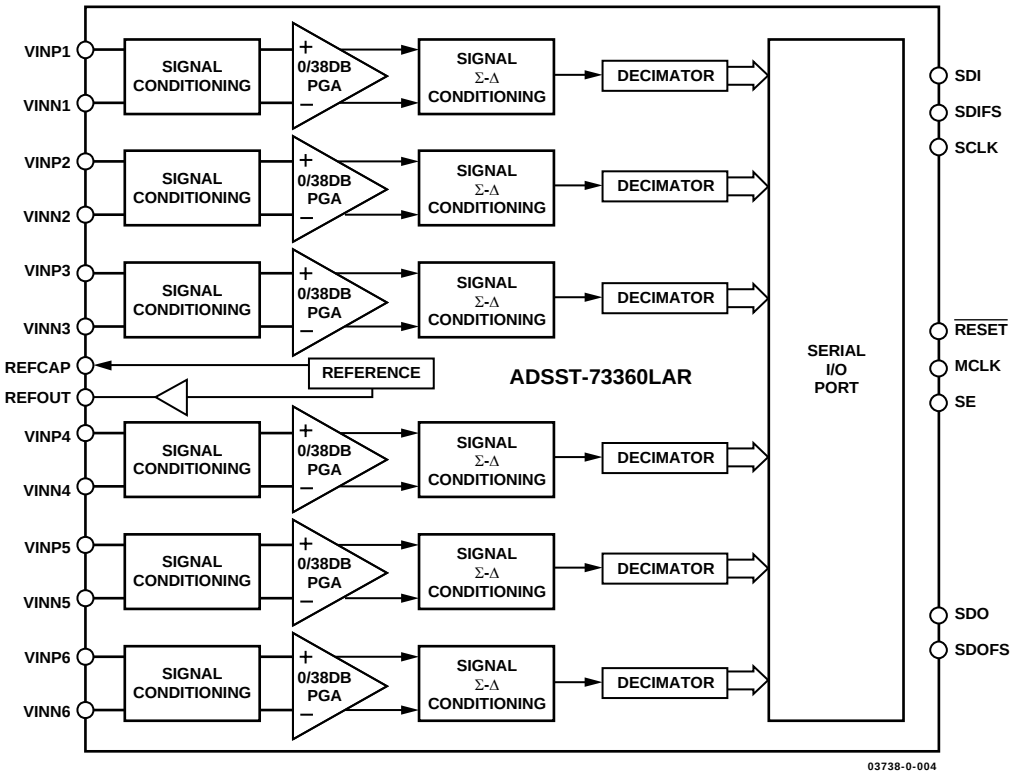

Figure 6. ADSST-73360LAR Functional Block Diagram

SPECIFICATIONS—ADSST-73360LAR

(AVDD = 2.7 V to 3.6 V, DVDD = 2.7 V to 3.6 V, DGND = AGND = 0 V, f_{MCLK} = 16.384 MHz, f_{SCLK} = 8.192 MHz, f_S = 8 kHz, T_A = T_{MIN} to T_{MAX}[1], unless otherwise noted.)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions
REFERENCE					
REFCAP					
Absolute Voltage, V_{REFCAP}	1.08	1.2	1.32	V	
REFCAP TC		50		ppm/°C	0.1 μF Capacitor Required from REFCAP to AGND2
REFOUT					
Typical Output Impedance		130		Ω	
Absolute Voltage, V_{REFOUT}	1.08	1.2	1.32	V	Unloaded
Minimum Load Resistance	1			kΩ	
Maximum Load Capacitance			100	pF	
ADC SPECIFICATIONS					
Maximum Input Range at VIN[2, 3]		1.578		V p-p	Measured Differentially
		–2.85		dBm	
Nominal Reference Level at VIN (0 dBm0)		1.0954		V p-p	Measured Differentially
		–6.02		dBm	
Absolute Gain					
PGA = 0 dB	–1.3		+0.6	dB	1.0 kHz
PGA = 38 dB	–0.8		+0.8	dB	1.0 kHz
Signal to (Noise + Distortion)					
PGA = 0 dB		76		dB	0 Hz to 4 kHz; f_S = 8 kHz
PGA = 0 dB	71	76		dB	0 Hz to 2 kHz; f_S = 8 kHz; f_{IN} = 60 kHz
PGA = 38 dB		58		dB	0 Hz to 4 kHz; f_S = 64 kHz
Total Harmonic Distortion					
PGA = 0 dB		–80	–71	dB	0 Hz to 2 kHz; f_S = 8 kHz; f_{IN} = 60 kHz
PGA = 38 dB		–64		dB	0 Hz to 2 kHz; f_S = 64 kHz; f_{IN} = 60 kHz
Intermodulation Distortion		–78		dB	PGA = 0 dB
Idle Channel Noise		–68		dB	PGA = 0 dB, f_S = 64 kHz; SCLK = 16 MHz
Crosstalk ADC-to-ADC		–95		dB	ADC1 at Idle; ADC2 to ADC6 Input Signal: 60 Hz
DC Offset	–30		+30	mV	PGA = 0 dB
Power Supply Rejection		–55		dB	Input Signal Level at AVDD and DVDD Pins 1.0 kHz, 100 mV p-p Sine Wave
Group Delay[4, 5]		25		μs	64 kHz Output Sample Rate
		50		μs	32 kHz Output Sample Rate
		95		μs	16 kHz Output Sample Rate
		190		μs	8 kHz Output Sample Rate
Input Resistance at VIN[2, 4]		25		kΩ[6]	DMCLK = 16.384 MHz
Phase Mismatch		0.15		Degrees	f_{IN} = 1 kHz
		0.01		Degrees	f_{IN} = 60 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions
FREQUENCY RESPONSE					
(ADC)[7] Typical Output Frequency (Normalized to f_S)					
0		0		dB	
0.03125		−0.1		dB	
0.0625		−0.25		dB	
0.125		−0.6		dB	
0.1875		−1.4		dB	
0.25		−2.8		dB	
0.3125		−4.5		dB	
0.375		−7.0		dB	
0.4375		−9.5		dB	
> 0.5		< −12.5		dB	
LOGIC INPUTS					
V_{INH}, Input High Voltage	V_{DD} − 0.8		V_{DD}	V	
V_{INL}, Input Low Voltage	0		0.8	V	
I_{IH}, Input Current			10	μA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUT					
V_{OH}, Output High Voltage	V_{DD} − 0.4		V_{DD}	V	$\|I_{OUT}\| \leq 100$ μA
V_{OL}, Output Low Voltage	0		0.4	V	$\|I_{OUT}\| \leq 100$ μA
Three-State Leakage Current	−10		+10	μA	
POWER SUPPLIES					
AVDD1, AVDD2	2.7		3.6	V	
DVDD	2.7		3.6	V	
IDD[8]					See Table 7

[1]Operating temperature range is as follows: −40°C to +85°C. Therefore, T_{MIN} = −40°C and T_{MAX} = +85°C.
[2]Test conditions: Input PGA set for 0 dB gain (unless otherwise noted).
[3]At input to sigma-delta modulator of ADC.
[4]Guaranteed by design.
[5]Overall group delay will be affected by the sample rate and the external digital filtering.
[6]The ADC's input impedance is inversely proportional to DMCLK and is approximated by: (4×10^{11})/DMCLK.
[7]Frequency response of the ADC measured with input at audio reference level (the input level that produces an output level of 0 dBm0), with 38 dB preamplifier bypassed and input gain of 0 dB.
[8]Test Conditions: no load on digital inputs, analog inputs ac-coupled to ground.

Table 7. Current Summary (AVDD = DVDD = 3.3 V)

Conditions	Digital Current, Max (mA)	SE	MCLK ON	Comments
ADCs Only On	25	1	Yes	REFOUT Disabled
REFCAP Only On	1.0	0	No	REFOUT Disabled
REFCAP and REFOUT Only On	3.5	0	No	
All Sections On	26.5	1	Yes	REFOUT Enabled
All Sections Off	1.0	1	Yes	MCLK Active Levels Equal to 0 V and DVDD
All Sections Off	0.05	0	No	Digital Inputs Static and Equal to 0 V or DVDD

The above values are in mA and are typical values, unless otherwise noted. MCLK = 16.384 MHz; SCLK = 16.384 MHz.

ABSOLUTE MAXIMUM RATINGS—ADSST-73360LAR

(T_A = 25°C unless otherwise noted)

Table 8.

Parameter	Rating
AVDD, DVDD to GND	–0.3 V to +4.6 V
AGND to DGND	–0.3 V to +0.3 V
Digital I/O Voltage to DGND	–0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND	–0.3 V to AVDD
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Maximum Junction Temperature	150°C
Thermal Impedance θ_{JA} (SOIC)	75°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS—ADSST-73360LAR

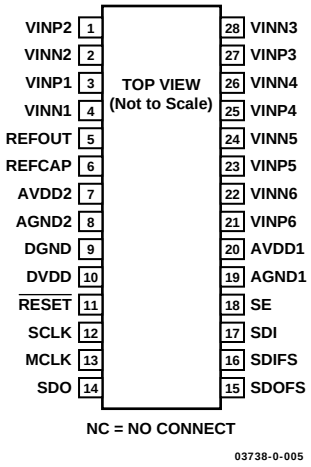

Figure 7. ADSST-73360LAR Pin Configuration—RW-28

PIN FUNCTION DESCRIPTIONS

Table 9.

Pin No.	Mnemonic	Function
1	VINP2	Analog Input to the Positive Terminal of Input Channel 2.
2	VINN2	Analog Input to the Negative Terminal of Input Channel 2.
3	VINP1	Analog Input to the Positive Terminal of Input Channel 1.
4	VINN1	Analog Input to the Negative Terminal of Input Channel 1.
5	REFOUT	Buffered Output of the Internal Reference, which has a nominal value of 1.2 V.
6	REFCAP	Reference Voltage for ADCs. A bypass capacitor to AGND2 of 0.1 μF is required for the on-chip reference. The capacitor should be fixed to this pin. The internal reference can be overdriven by an external reference connected to this pin if required.
7	AVDD2	Analog Power Supply Connection.
8	AGND2	Analog Ground/Substrate Connection.
9	DGND	Digital Ground/Substrate Connection.
10	DVDD	Digital Power Supply Connection.
11	$\overline{\text{RESET}}$	Active Low Reset Signal. This input resets the entire chip, resetting the control registers and clearing the digital circuitry.
12	SCLK	Output Serial Clock whose rate determines the serial transfer rate to/from the ADSST-73360LAR. It is used to clock data or control information to and from the serial port (SPORT). The frequency of SCLK is equal to the frequency of the master clock (MCLK) divided by an integer number that is the product of the external master clock rate divider and the serial clock rate divider.
13	MCLK	Master Clock Input. MCLK is driven from an external clock signal.
14	SDO	Serial Data Output of the ADSST-73360LAR. Both data and control information may be output on this pin and are clocked on the positive edge of SCLK. SDO is in three-state when no information is being transmitted and when SE is low.
15	SDOFS	Framing Signal Output for SDO Serial Transfers. The frame sync is one bit wide and it is active one SCLK period before the first bit (MSB) of each output word. SDOFS is referenced to the positive edge of SCLK. SDOFS is in three-state when SE is low.
16	SDIFS	Framing Signal Input for SDI Serial Transfers. The frame sync is one bit wide and it is valid one SCLK period before the first bit (MSB) of each input word. SDIFS is sampled on the negative edge of SCLK and is ignored when SE is low.
17	SDI	Serial Data Input of the ADSST-73360LAR. Both data and control information may be input on this pin and are clocked on the negative edge of SCLK. SDI is ignored when SE is low.

Pin No.	Mnemonic	Function
18	SE	SPORT Enable. Asynchronous input enable pin for the SPORT. When SE is set low by the DSP, the output pins of the SPORT are three-stated and the input pins are ignored. SCLK is also disabled internally in order to decrease power dissipation. When SE is brought high, the control and data registers of the SPORT are at their original values (before SE was brought low); however, the timing counters and other internal registers are at their reset values.
19	AGND1	Analog Ground Connection.
20	AVDD1	Analog Power Supply Connection.
21	VINP6	Analog Input to the Positive Terminal of Input Channel 6.
22	VINN6	Analog Input to the Negative Terminal of Input Channel 6.
23	VINP5	Analog Input to the Positive Terminal of Input Channel 5.
24	VINN5	Analog Input to the Negative Terminal of Input Channel 5.
25	VINP4	Analog Input to the Positive Terminal of Input Channel 4.
26	VINN4	Analog Input to the Negative Terminal of Input Channel 4.
27	VINP3	Analog Input to the Positive Terminal of Input Channel 3.
28	VINN3	Analog Input to the Negative Terminal of Input Channel 3.

GROUNDING AND LAYOUT

Since the analog inputs to the ADSST-73360LAR are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The analog and digital supplies of the ADSST-73360LAR are independent and separately pinned out to minimize coupling between analog and digital sections of the device. The digital filters on the encoder section provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filters also remove noise from the analog inputs, provided the source does not saturate the analog modulator. However, because the resolution of the ADSST-73360LAR's ADC is high and the noise levels from the ADSST-73360LAR are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the ADSST-73360LAR should be designed in such a way that the analog and digital sections are separated and confined to certain sections of the board. The ADSST-73360LAR pin configuration offers a major advantage in that its analog and digital interfaces are connected on opposite sides of the package. This facilitates the use of ground planes that can be easily separated, as shown in Figure 8.

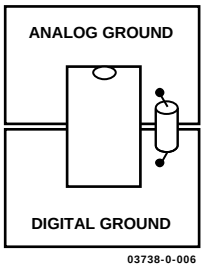

Figure 8. Ground Plane Layout

A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined in only one place. If this connection is close to the device, it is recommended to use a ferrite bead inductor as shown in Figure 9.

Avoid running digital lines under the device for they will couple noise onto the die. The analog ground plane should be enabled to run under the ADSST-73360LAR to avoid noise coupling. The power supply lines to the ADSST-73360LAR should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply lines. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feed-through through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the other side.

Good decoupling is important when using high speed devices. All analog and digital supplies should be decoupled to AGND and DGND, respectively, with 0.1 μF ceramic capacitors in parallel with 10 μF tantalum capacitors. To achieve the best from these decoupling capacitors, they should be placed as close as possible to the device, ideally right up against it. In systems where a common supply voltage is used to drive both the AVDD and DVDD of the ADSST-73360LAR, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the ADSST-73360LAR and AGND, and the recommended digital supply decoupling capacitors between the DVDD pin and DGND.

POWER-UP INITIALIZATION AND DATA FROM THE ADSST-SALEM-3T

The ADSST-SALEM-3T-EV boot loads the code from the nonvolatile flash memory as shown in the block diagram of a functional meter in Figure 1. The configuration and calibration data also gets loaded from the nonvolatile memory. For further details on boot loading, refer to the ADSST-SALEM-3T-DK (Developer's Kit) User Manual. The user manual also describes various commands for instantaneous and computed parameters.

VOLTAGE AND CURRENT SENSING

Figure 9 shows the input section for the voltage and current sections. Based on the voltage and current values, the GUI software in the ADSST-SALEM-3T-DK computes the values of resistors R1, R2, and R3. The closest available values to those calculated by the GUI software should be selected and used.

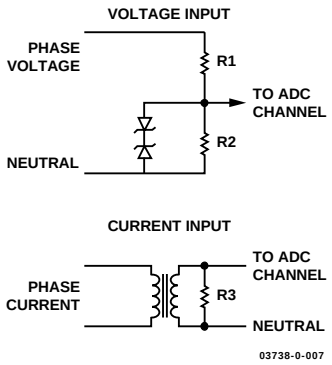

Figure 9. Input Section

The ADSST-73360LAR has a peak-to-peak input range of V_{REF} – (V_{REF} × 0.6525) to V_{REF} + (V_{REF} × 0.6525); for V_{REF} = 2.5 V, this is 0.856 V to 4.14 V p-p. This limit defines the resistance network on the potential circuits and the burden resistance on the secondary side of the CT. Since the ADSST-73360LAR is a unipolar ADC, the ac potential and current signals have to be offset by some dc level. The reference design has a dc offset of 2.5 V. This limits the peak-to-peak signal range of potential and current to 3.28 V p-p or 1.16 V rms.

Potential Section

The selection of the potential divider circuit should be such that it can:

- Handle high surge voltages
- Have minimum VA burden
- Give approximately 1 V peak headroom to accommodate overvoltages.

Current Section

The selection of CT ratio and burden resistance should be such that it can:

- Handle the complete dynamic range for the current signal input.
- Give approximately 1 V peak headroom to accommodate loads with high crest factors.

The reference design has a CT with a turns ratio of 1:2500 and burden resistance of 82 Ω. This generates 0.656 V rms or 0.928 V peak at 20 A current. This leaves enough margin for current pulses or low crest factor loads, such as SMPS. The maximum current can be up to 32.768 A.

ACCURACY OF REFERENCE DESIGN USING THE ADSST-SALEM-3T CHIPSET

Overall Accuracy, Power, and Energy Measurement

The accuracy figures are measured under typical specified conditions, unless otherwise indicated.

Table 10. Test Conditions for Reference Design Using a µ Metal CT of Class 0.5 Accuracy

Parameter	Nominal Value
Nominal Voltage (Phase to Neutral) V_N	V_N = 230 V ± 1%
Maximum Voltage (Phase to Neutral)	300 V
Nominal Current	I_N = 5 A
Maximum Current I_{MAX}	I_{MAX} = 20 A
Frequency	F_N = 50 Hz/60 Hz ± 10%
Temperature	23 ± 2°C

Table 11. Maximum Error (Power and Energies)

Current	Voltage	PF	Min	Typ	Max	Unit
0.01 $I_N \le I < 0.05\ I_N$	V_N	1.0		±0.1	±0.2	%
0.05 $I_N \le I < I_{MAX}$	V_N	1.0		±0.1	±0.2	%
0.02 $I_N \le I < 0.1\ I_N$	V_N	0.5 Lagging		±0.15	±0.35	%
		0.8 Leading		±0.15	±0.35	%
0.05 $I_N \le I < I_{MAX}$	V_N	0.5 Lagging		±0.1	±0.2	%
		0.8 Leading		±0.1	±0.2	%

Table 12. Unbalanced Load Error

Current	Voltage	PF	Min	Typ	Max	Unit
0.05 $I_N \le I \le I_{MAX}$	V_N	1.0		±0.15	±0.2	%
0.1 $I_N \le I \le I_{MAX}$	V_N	0.5 Lagging		±0.15	±0.2	%

Table 13. Voltage Variation Error

Voltage	Current	PF	Min	Typ	Max	Unit
V_N ± 10%	0.05 $I_N \le I \le I_{MAX}$	1.0		±0.05	±0.1	%
V_N ± 10%	0.1 $I_N \le I \le I_{MAX}$	0.5 Lagging		±0.05	±0.1	%

Table 14. Frequency Variation Errors

Frequency	Current	PF	Min	Typ	Max	Unit
f_N ± 10%	0.05 $I_N \le I \le I_{MAX}$	1.0		±0.05	±0.1	%
f_N ± 10%	0.1 $I_N \le I \le I_{MAX}$	0.5 Lagging		±0.05	±0.1	%

Table 15. Harmonic Distortion Error

Current	Current	Min	Typ	Max	Unit
10% of 3rd Harmonic	0.05 $I_N \le I \le I_{MAX}$		±0.05	±0.1	%

Table 16. Reverse Phase Sequence Error

Current	Voltage	Min	Typ	Max	Unit
0.1 I_N	V_N			±0.05	%

Table 17. Voltage Unbalance Error

Current	Voltage	Min	Typ	Max	Unit
I_N	V_N + 15% V		±0.1	±0.2	%

Table 18. Starting Current

Min	Typ	Max	Unit
	0.07	0.1	% of I_N

OUTLINE DIMENSIONS

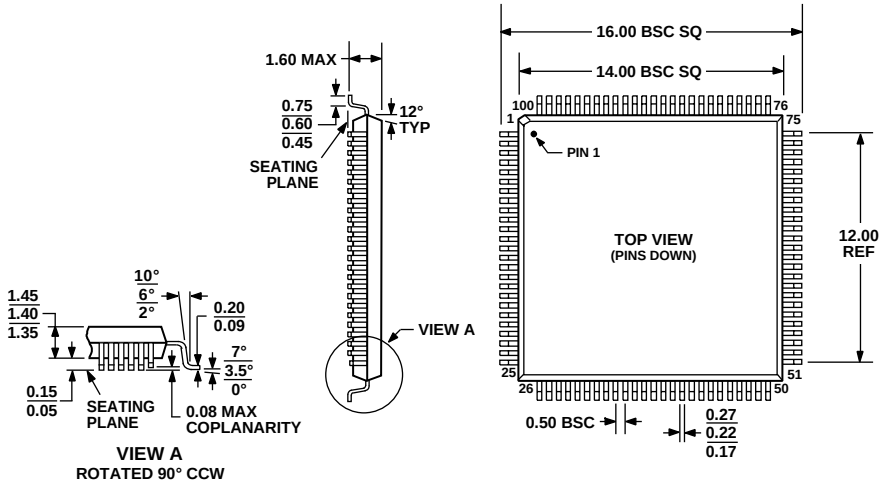

Figure 10. 100-Lead Low Profile Quad Flat Package [LQFP]
(ST-100)
Dimensions shown in millimeters

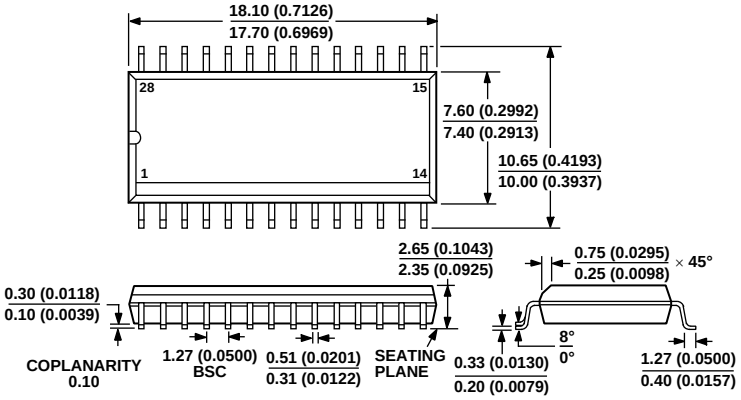

Figure 11. 28-Lead Standard Small Outline Package [SOIC]
Wide Body
(RW-28)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Part Number[1]	Temperature Range	Processors Included	Package
ADSST-EM-3040	0°C to +70°C	ADSST-2185MKST-300	ST-100
		ADSST-73360LAR	RW-28
ADSST-EM-3041	−25°C to +85°C	ADSST-2185MBST-266	ST-100
		ADSST-73360LAR	RW-28

[1] For developer's kit, order ADSST-SALEM-3T-DK.

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